

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 08/650,719

Filing Date: May 20, 1996

Title: ASYNCHRONOUSLY-ACCESSIBLE MEMORY DEVICE WITH MODE SELECTION CIRCUITRY FOR BURST OR PIPELINED OPERATION

Page 2

Dkt: 303.623US1

different from claim 46. Applicant believes that once the Office has an opportunity to review the cited portions in the specification as discussed above, the Office will concur. Reconsideration and withdrawal of the objection is respectfully requested.

§102 Rejection of the Claims

Claims 1-9, 33-35, 46, 48-50, and 59-64 were rejected under 35 USC § 102(b) as being anticipated by Manning (U.S. Patent No. 5,610,864).

The statutory language of section 102(b) provides that "[a] person shall be entitled to a patent unless ... the invention was patented ... more than one year prior to the date of the application for patent in the United States." The patent date of Manning is insufficient to support the rejection under section 102(b). Thus, the rejection is improper. Reconsideration of the rejection is respectfully requested.

The MPEP requires that "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." See MPEP sec. 2131. The Office fails to show that Manning discusses the identical invention, which is claimed in applicant's application.

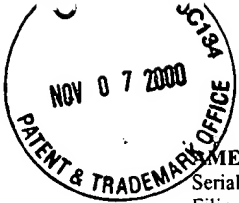
The Office has failed to produce a *prima facie* case of anticipation. For example, applicant cannot find and the Office has failed to show where Manning discusses selecting between a burst mode and a pipelined mode.. The Office noted that Manning discusses a "pipelined architecture" at column 5, lines 43-50. And the Office indicated that Manning discusses "switching between burst EDO and standard EDO modes of operation" at column 6, lines 14-22, and "selecting between standard fast page mode (non-EDO) and burst mode" at column 7, lines 44-55.

Applicant believes that the Office misapprehends the Manning reference, and applicant would like to clarify. Applicant has explained that EDO mode is a mode that provides a longer period of time for when data is valid at the outputs of a DRAM. See applicant's specification at page 3, lines 19-21. Applicant has discussed that fast page mode is a mode that uses a row address strobe to latch a row address portion of a DRAM address. See applicant's specification at page 2, lines 12-13. Applicant has also explained that pipelined mode is a mode that divides address information into operational times such that the address information can be provided from an external source as a stream of data. See applicant's specification at page 8, lines 1-13.

Applicant cannot find where Manning discusses that these mode are interchangeable. The Office indicated that "Manning discloses switching between fast page pipeline and burst pipeline." First, applicant is unclear about what is a fast page pipeline or a burst pipeline; applicant cannot find them in Manning. Second, the Office is correct in that Manning indicated that "[t]he current invention include a pipelined architecture." See Manning at column 5, lines 43-44. But this should be read in context of Manning's Field of the Invention: "This invention relates more specifically to circuits and methods for controlling memory write cycles in burst access memory devices." See Manning at column 1, lines 11-13. Compare to the applicant's Field of the Invention: "This invention relates ... more particularly to dynamic random access memory, which is switch selectable between burst and pipelined modes." Applicant cannot find, and the Office has failed to show, a single instance where Manning discusses burst and pipelined modes together.

In short, what is discussed by Manning is not identical to the subject matter of the present invention as required by the MPEP, and therefore, the rejection is improper. Reconsideration and allowance of claims 1-9, 33-35, 46, 48-50, and 59-64 is respectfully requested.

Applicant has also studied the cited reference (Rosich, U.S. Patent No. 5,587,964), but does not believe that Rosich precludes allowance of the claims 1-9, 33-35, 46, 48-50, and 59-64. Reconsideration is respectfully requested.



AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 08/650,719

Filing Date: May 20, 1996

Title: ASYNCHRONOUSLY-ACCESSIBLE MEMORY DEVICE WITH MODE SELECTION CIRCUITRY FOR BURST OR PIPELINED OPERATION

Page 4

Dkt: 303.623US1

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 371-2129 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JEFFREY S. MAILLOUX ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938

Minneapolis, MN 55402

(612) 371-2129

Date November 3, 2000

By

Dinh C.P. Chu

Reg. No. 41,676

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner of Patents, Washington, D.C. 20231 on November 3, 2000.

Name

Tina Pugh

Signature